library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use ieee.numeric\_std.all;

use ieee.std\_logic\_unsigned.all;

entity tb\_8Mhz\_Sample is

-- Port ( );

end tb\_8Mhz\_Sample;

architecture Behavioral of tb\_8Mhz\_Sample is

component cic

generic(CI\_SIZE : integer; -- cic input data width

CO\_SIZE : integer; -- cic output data width

STAGES : integer);

port (clk : in std\_logic; -- system clock (80 Mhz)

ce : in std\_logic; -- clock enable

ce\_r : in std\_logic; -- decimated clock by factor of 5 used in comb section

rst : in std\_logic; -- system reset

d : in std\_logic\_vector (CI\_SIZE-1 downto 0); -- input data

q : out std\_logic\_vector (CO\_SIZE-1 downto 0)); -- output data

end component;

signal temp1:std\_logic:='0';

signal temp:std\_logic\_vector(2 downto 0):="000";

signal din:std\_logic\_vector(19 downto 0);

signal dout:std\_logic\_vector(29 downto 0);

signal ce\_r,clk:std\_logic;

signal ce:std\_logic:='0';

signal rst:std\_logic:='0';

constant clock\_period:time:=12.5 ns;

begin

rst<='1','0' after 12.5 ns ;

ce<='1' after 12.5 ns;

ce\_r<=temp1;

u1:cic generic map(CI\_SIZE=>20,CO\_SIZE=>30,STAGES=>5)

port map(clk=>clk,ce=>ce,ce\_r=>ce\_r,rst=>rst,d=>din, q=>dout);

din\_steady :process

begin

--8 Mhz

--wait for 12.5 ns;

--din <= std\_logic\_vector(to\_signed(0,20));

--wait for 12.5 ns;

--din <= std\_logic\_vector(to\_signed(308168,20));

--wait for 12.5 ns;

--din <= std\_logic\_vector(to\_signed(498627,20));

--wait for 12.5 ns;

--din <= std\_logic\_vector(to\_signed(498627,20));

--wait for 12.5 ns;

--din <= std\_logic\_vector(to\_signed(308168,20));

--wait for 12.5 ns;

--din <= std\_logic\_vector(to\_signed(0,20));

--wait for 12.5 ns;

--din <= std\_logic\_vector(to\_signed(-308168,20));

--wait for 12.5 ns;

--din <= std\_logic\_vector(to\_signed(-498627,20));

--wait for 12.5 ns;

--din <= std\_logic\_vector(to\_signed(-498627,20));

--16 MHz

-- wait for 12.5 ns;

-- din <= std\_logic\_vector(to\_signed(0,20));

-- wait for 12.5 ns;

-- din <= std\_logic\_vector(to\_signed(498627,20));

-- wait for 12.5 ns;

-- din <= std\_logic\_vector(to\_signed(308168,20));

-- wait for 12.5 ns;

-- din <= std\_logic\_vector(to\_signed(-30816,20));

-- wait for 12.5 ns;

-- din <= std\_logic\_vector(to\_signed(-498627,20));

-- wait for 12.5 ns;

-- din <= std\_logic\_vector(to\_signed(0,20));

--24 Mhz

wait for 12.5 ns;

din <= std\_logic\_vector(to\_signed(0,20));

wait for 12.5 ns;

din <= std\_logic\_vector(to\_signed(498627,20));

wait for 12.5 ns;

din <= std\_logic\_vector(to\_signed(308168,20));

wait for 12.5 ns;

din <= std\_logic\_vector(to\_signed(-30816,20));

end process;

clock:process

begin

clk<='0';

wait for clock\_period/2;

clk<= not clk;

wait for clock\_period/2;

end process;

process(clk)

begin

if rising\_edge(clk) then

temp<=temp+1;

if (temp="100") then

temp1<=not temp1;

elsif (temp="101") then

temp1<=not temp1;

temp<="001";

end if;

end if;

end process;

end Behavioral;